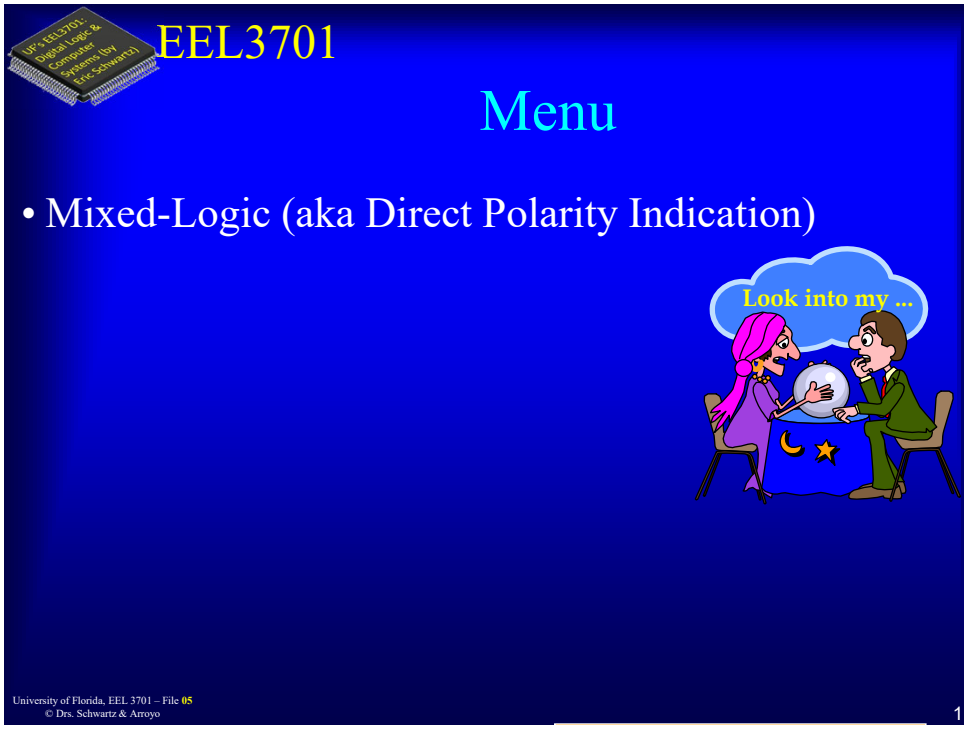
EEL3701
Menu
• Mixed-Logic (aka Direct Polarity Indication)
Look into my ...
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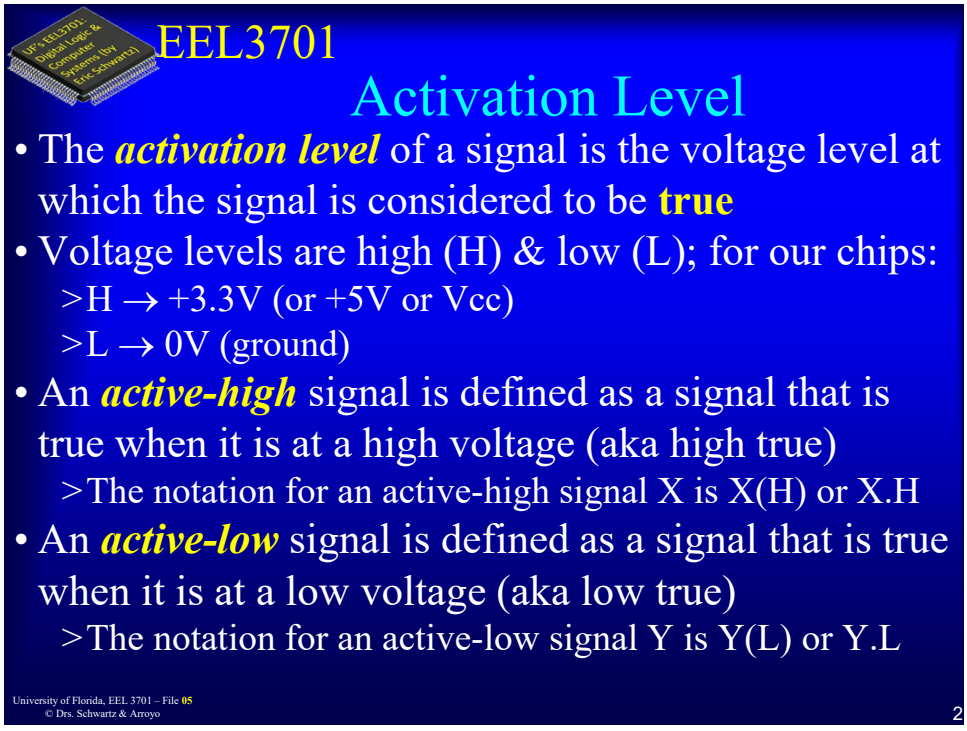
1

1


EEL3701
Activation Level
• The activation level of a signal is the voltage level at which the signal is considered to be true
• Voltage levels are high (H) & low (L); for our chips:
>H → +3.3V (or +5V or Vcc)
>L → 0V (ground)
• An active-high signal is defined as a signal that is true when it is at a high voltage (aka high true)
>The notation for an active-high signal X is X(H) or X.H
• An active-low signal is defined as a signal that is true when it is at a low voltage (aka low true)
>The notation for an active-low signal Y is Y(L) or Y.L
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2

EEL3701

Voltage Levels

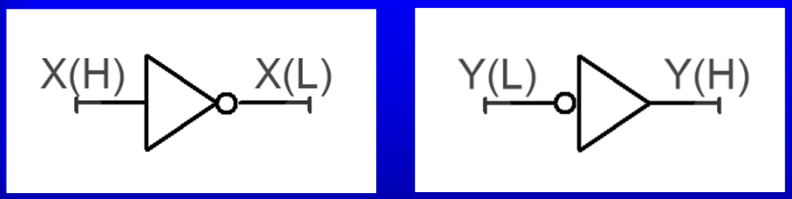
- For other type chips the voltages may be
  - >For serial EIA-232: +12V/-12V
  - >Other common high voltage (with low = 0V)
    - 2.5V, 2.4V, 1.8V, 1.5V, 1.35V, 1.25V, 1.2V

3

EEL3701

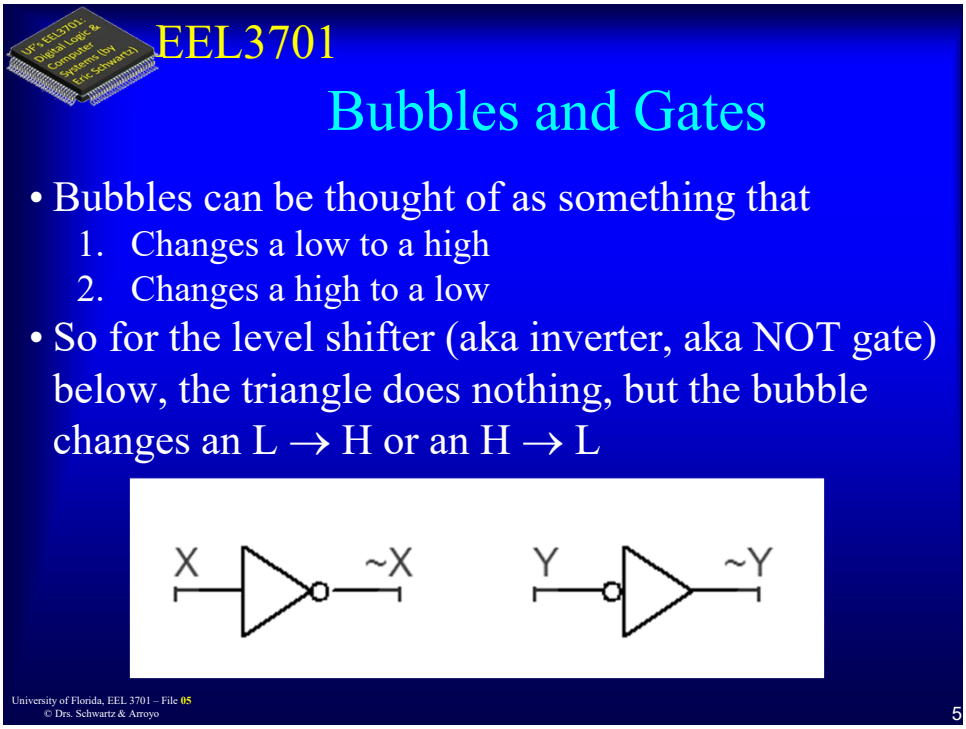
Level Shifters

- Level shifters change the activation level of a signal from high to low or from low to high



- **Logically**, a level shifter does **nothing** to the signal
  - >If a signal is T (F) at the input side it is all T (F) at the output
  - >(**Electrically**, level shifter **complements**, H↔L)

4


EEL3701
Bubbles and Gates
• Bubbles can be thought of as something that
1. Changes a low to a high
2. Changes a high to a low
• So for the level shifter (aka inverter, aka NOT gate) below, the triangle does nothing, but the bubble changes an L → H or an H → L
X
~X
Y
~Y
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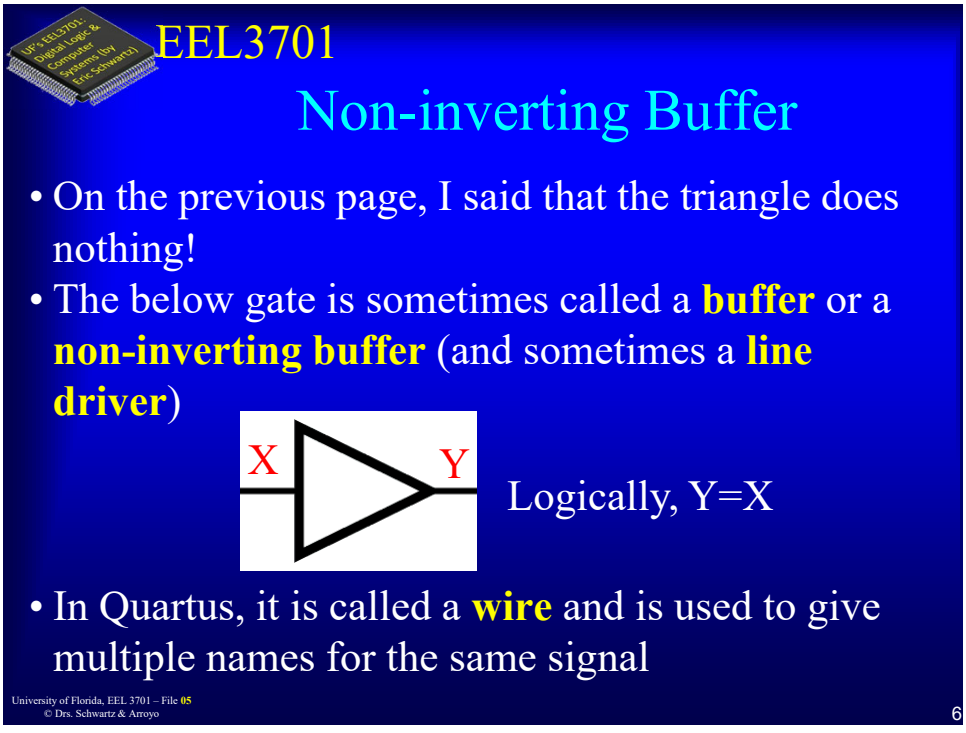
EEL3701
Non-inverting Buffer
• On the previous page, I said that the triangle does nothing!
• The below gate is sometimes called a buffer or a non-inverting buffer (and sometimes a line driver)
X
Y
Logically, Y=X
• In Quartus, it is called a wire and is used to give multiple names for the same signal
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A Little Boolean Algebra

Simple Boolean Algebra:

- Let X=/A
- If Y=/X, the Y=/(/A)=A
- In words:
  "The complement of the complement of A is A."

- When the bubbles are matched (i.e., there is no mismatch), **there is no complement**!

EEL3701

Direct Polarity Indication (Mixed-Logic)

- External logic states -vs- internal logic states
  - > **Logically**, a bubble has no effect (i.e., it only effects the activation level)
  - > Externally, you must specify signal activation levels, e.g., A(L) or A.L, B(H) or B.H
  - > Internally
    - – Match output activation-levels to input activation-level of gates (specified by bubbles)
    - – Then forget about activation levels!

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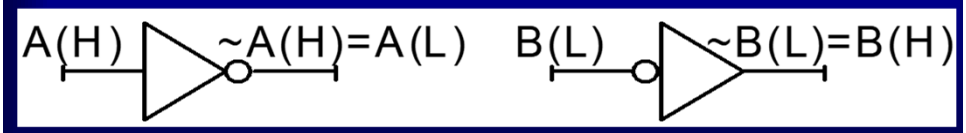
Mixed-Logic

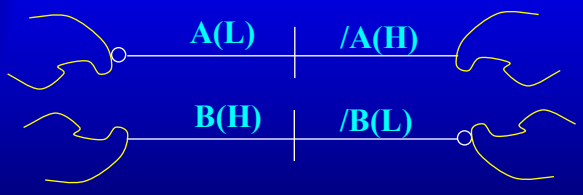
- At the input and output of a gate, **bubble ➔ active-low** and **non-bubble ➔ active-high**
- **Match** bubble to bubble or non-bubble to non-bubble, then variable unchanged (i.e., no complement)
- **Mismatch** in bubble/non-bubble means **complement**, *i.e.*, A(L)=/A(H), B(H)=/B(L)



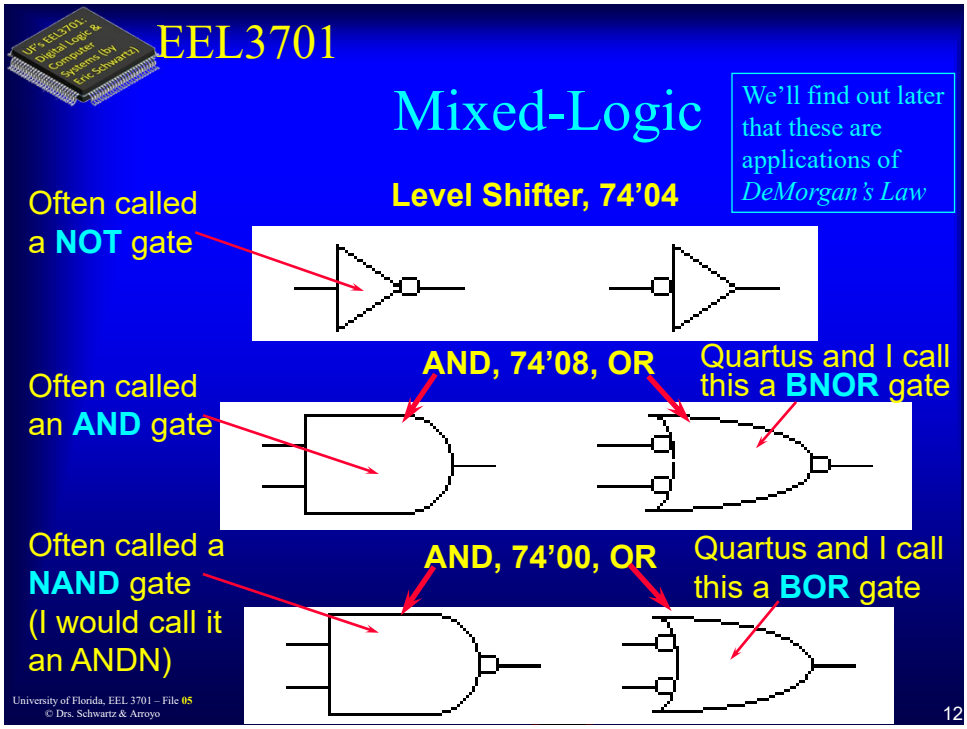
EEL3701

Mixed-Logic

- The **voltage** on a wire does **not** change (due to a bubble on an end), but the **logical** interpretation changes according to the equations: A(L)=/A(H) and **B(H)=/B(L)**



- Now we don't draw the vertical lines, but keep it in our heads that **mismatch ⇒ not**


EEL3701
Mixed-Logic
We'll find out later that these are applications of DeMorgan's Law
Level Shifter, 74'04
Often called a NOT gate
AND, 74'08, OR
Quartus and I call this a BNOR gate
Often called an AND gate
AND, 74'00, OR
Quartus and I call this a BOR gate
Often called a NAND gate (I would call it an ANDN)
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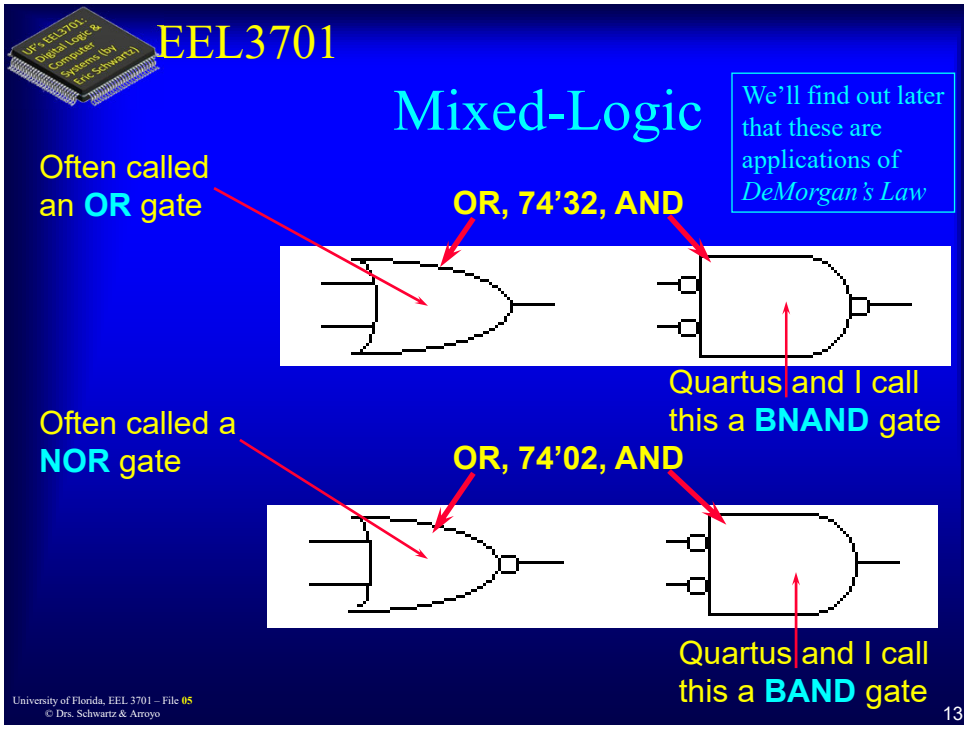
EEL3701
Mixed-Logic
We'll find out later that these are applications of DeMorgan's Law
Often called an OR gate
OR, 74'32, AND
Quartus and I call this a BNAND gate
Often called a NOR gate
OR, 74'02, AND
Quartus and I call this a BAND gate
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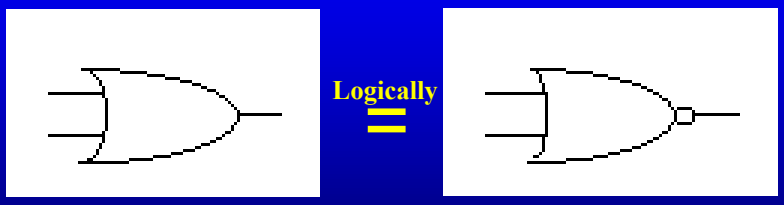
Mixed-Logic

- **Logically**, bubbles have **no** effect
  - >Ex: An OR gate is an OR gate is an OR gate



- (**Electrically**, bubbles **have** an effect)

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Mixed-Logic Example 1

(AND, OR, NOT)

Ex: X=A*B + /C (Only use 74'08, 74'32, 74'04)
Active-high: B, C Active-low: A, X

Procedure:

- Draw I/O with activation levels
- Draw gates near I/O to match equation (1 for 1 with ANDs and ORs, no NOTs)
- Fill in input and output bubbles and level shifters
- Fill in internal bubbles (and level shifters, if needed) and deal with complements

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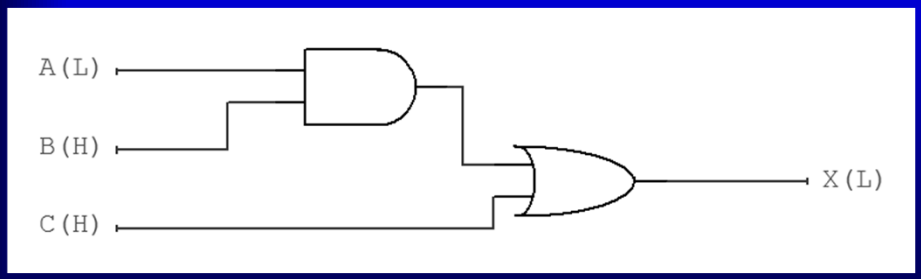
Mixed-Logic Example 1

Ex: X=A*B + /C (Only use 74'08, 74'32, 74'04)
Active-high: B, C Active-low: A, X

- Draw I/O with activation levels
- Draw gates near I/O to match equation



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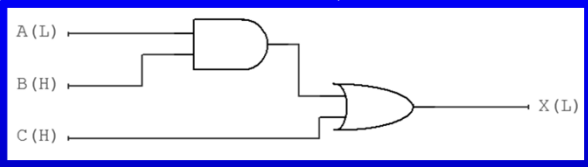
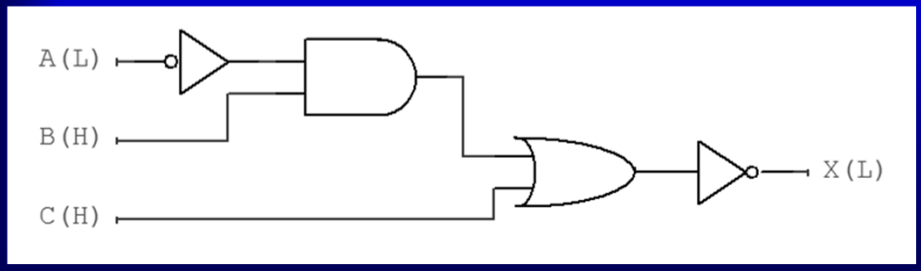
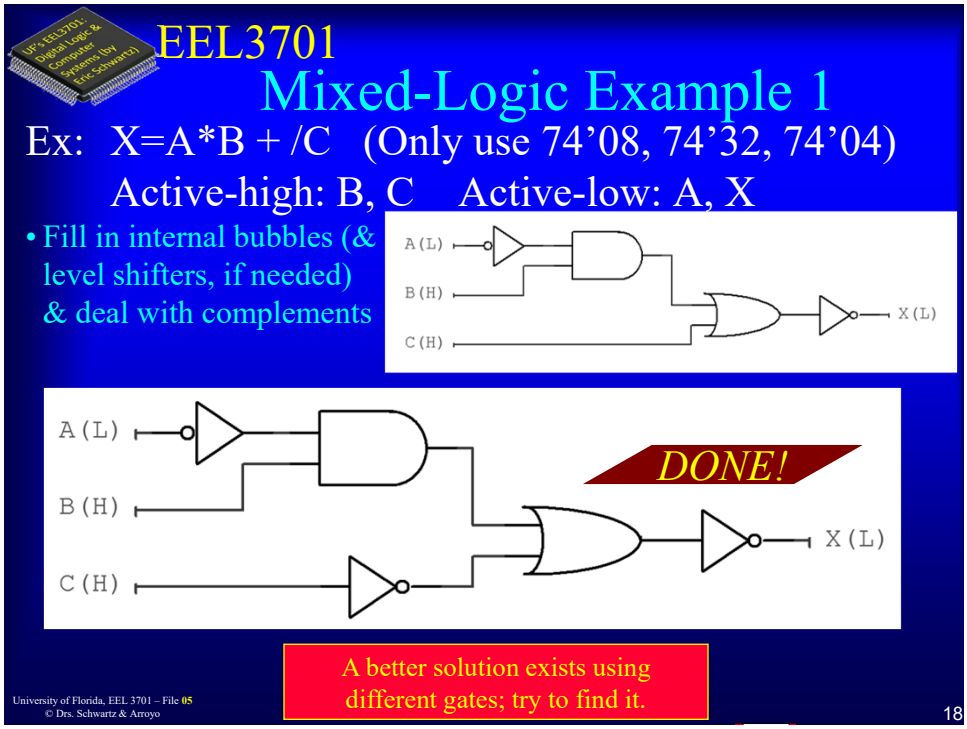
Mixed-Logic Example 1

Ex: X=A*B + /C (Only use 74'08, 74'32, 74'04)
Active-high: B, C Active-low: A, X

- Fill in input and output bubbles and level shifters






EEL3701
Mixed-Logic Example 1
Ex: X=A*B + /C (Only use 74'08, 74'32, 74'04)
Active-high: B, C Active-low: A, X
• Fill in internal bubbles (& level shifters, if needed) & deal with complements
A(L)
B(H)
C(H)
X(L)
A(L)
B(H)
C(H)
X(L)
DONE!
A better solution exists using different gates; try to find it.
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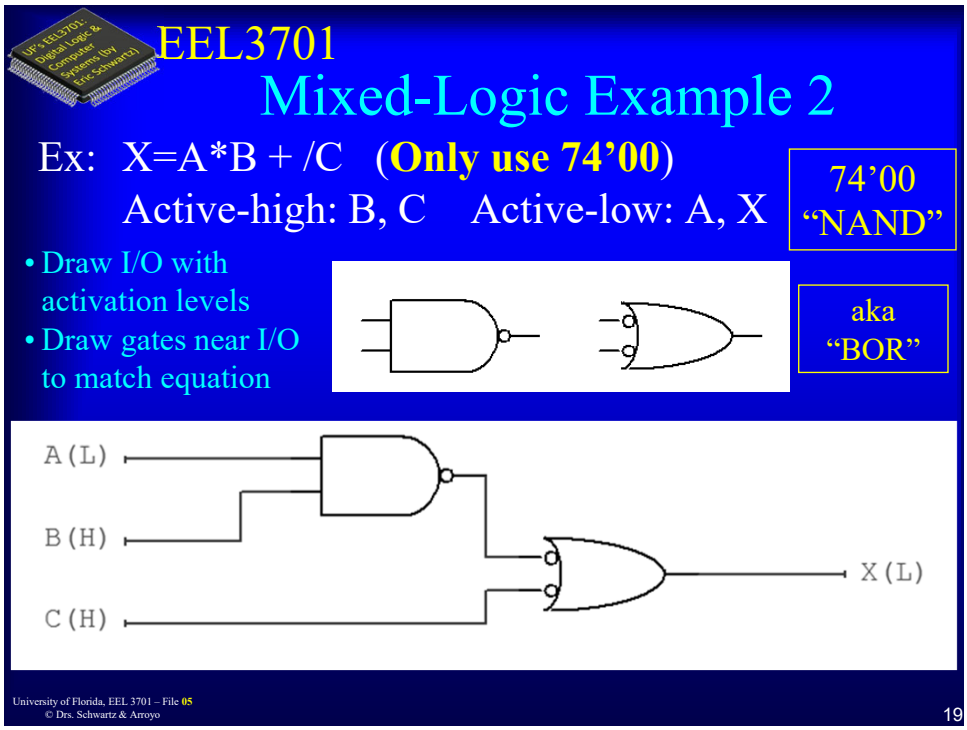
EEL3701
Mixed-Logic Example 2
Ex: X=A*B + /C (Only use 74'00)
Active-high: B, C Active-low: A, X
74'00 "NAND"
• Draw I/O with activation levels
• Draw gates near I/O to match equation
aka "BOR"
A(L)
B(H)
C(H)
X(L)
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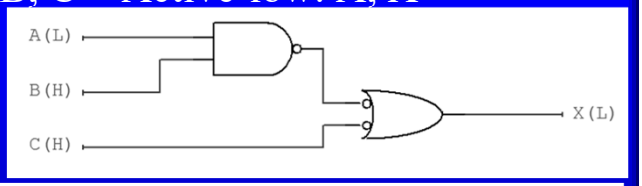
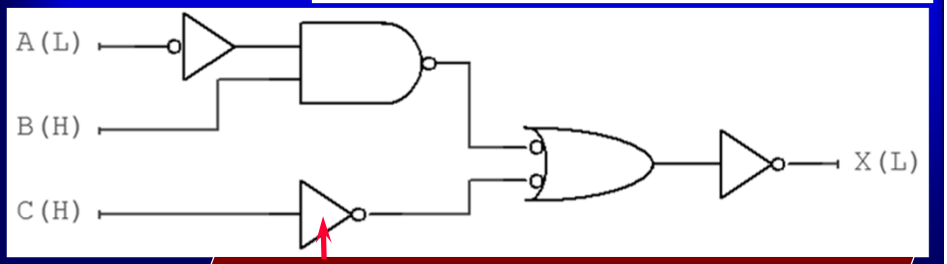
Mixed-Logic Example 2

Ex: X=A*B + /C **(Only use 74'00)**

Active-high: B, C Active-low: A, X

- Fill in input and output bubbles and level shifters





I normally would **not** put this level-shifter here in anticipation of the next step

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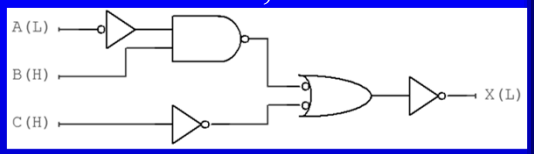
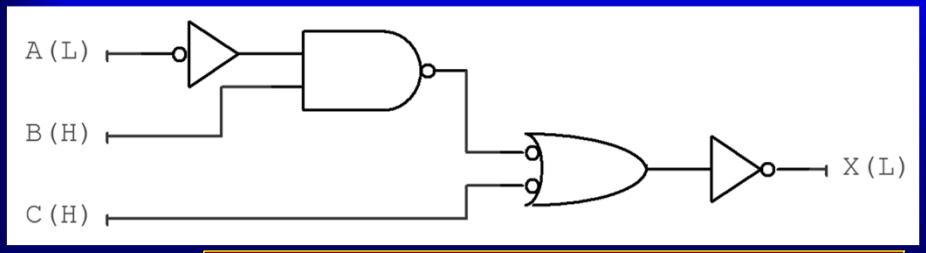
Mixed-Logic Example 2

Ex: X=A*B + /C **(Only use 74'00)**

Active-high: B, C Active-low: A, X

- Fill in internal bubbles (& level shifters, if needed) and deal with complements.





But I said **only** use NAND gates. We used two level shifters.

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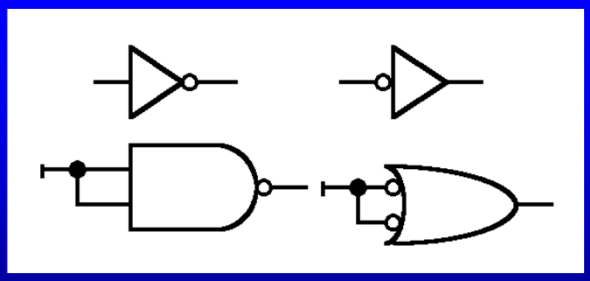
Level Shifter Equivalents using a NAND gate

- Can replace a level shifters in the example with any of the two NAND gate circuits shown
- The left column converts signals from active-high to active-low
- The right column converts from active-low to active-high.



Demo with LogicWorks

You can do the same things with NORs. **Do it at home!**

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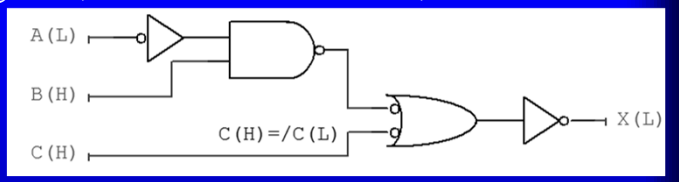
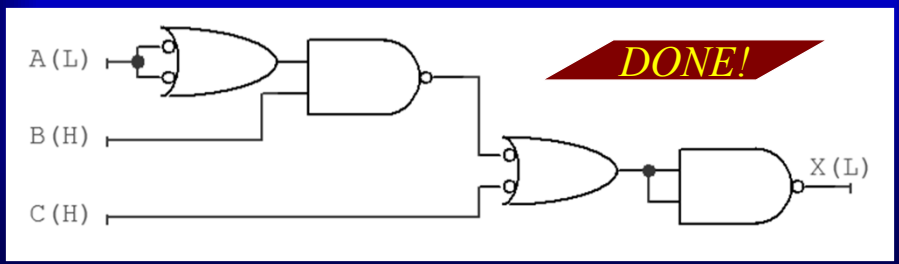
Mixed-Logic Example 2

Ex: X=A*B + /C **(Only use 74'00)**

Active-high: B, C Active-low: A, X

- Replace inverters with appropriate available gates





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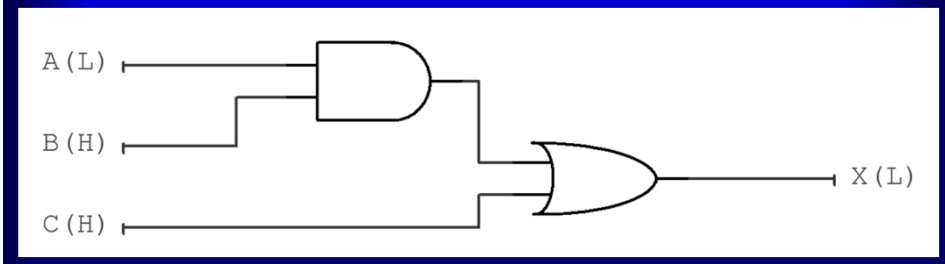
Mixed-Logic Example 3

Real gates: all **inputs** have **same** activation levels

Ex: X=A*B + /C (Use **anything real!**)

Active-high: B, C Active-low: A, X

- Draw I/O with activation levels
- Draw gates near I/O to match equation



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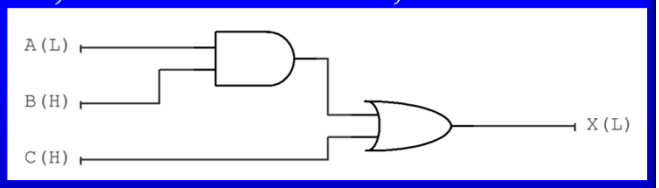
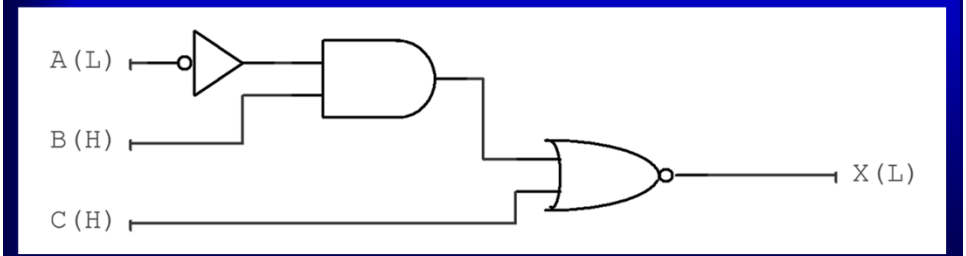
Mixed-Logic Example 3

Ex: X=A*B + /C (Use **anything real!**)

Active-high: B, C Active-low: A, X

- Fill in input and output bubbles and level shifters





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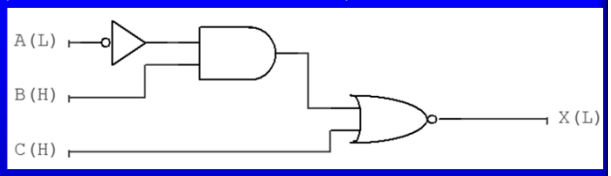
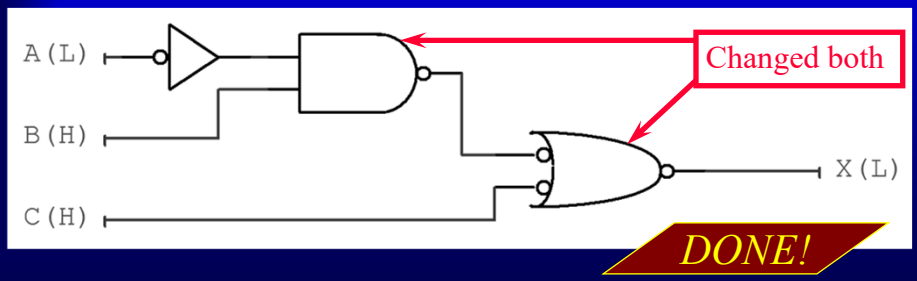
Mixed-Logic Example 3

Ex: X=A*B + /C (Use **anything real!**)

Active-high: B, C Active-low: A, X

- Fill in internal bubbles (& level shifters, if needed) and deal with complements





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Mixed-Logic Example 4

Ex: X=A*B + /C (Use **anything real!**)

Choose **ANY** activation levels that minimizes the number of gates

Solve this Live!

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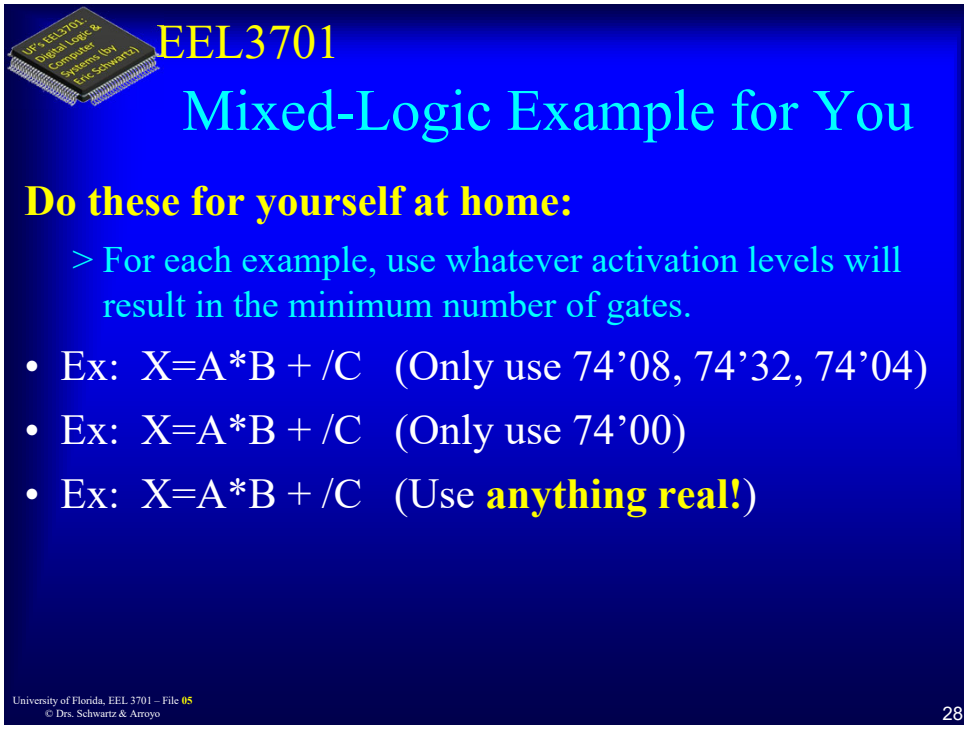
EEL3701
Mixed-Logic Example for You
Do these for yourself at home:
> For each example, use whatever activation levels will result in the minimum number of gates.
• Ex: X=A*B + /C (Only use 74'08, 74'32, 74'04)
• Ex: X=A*B + /C (Only use 74'00)
• Ex: X=A*B + /C (Use anything real!)
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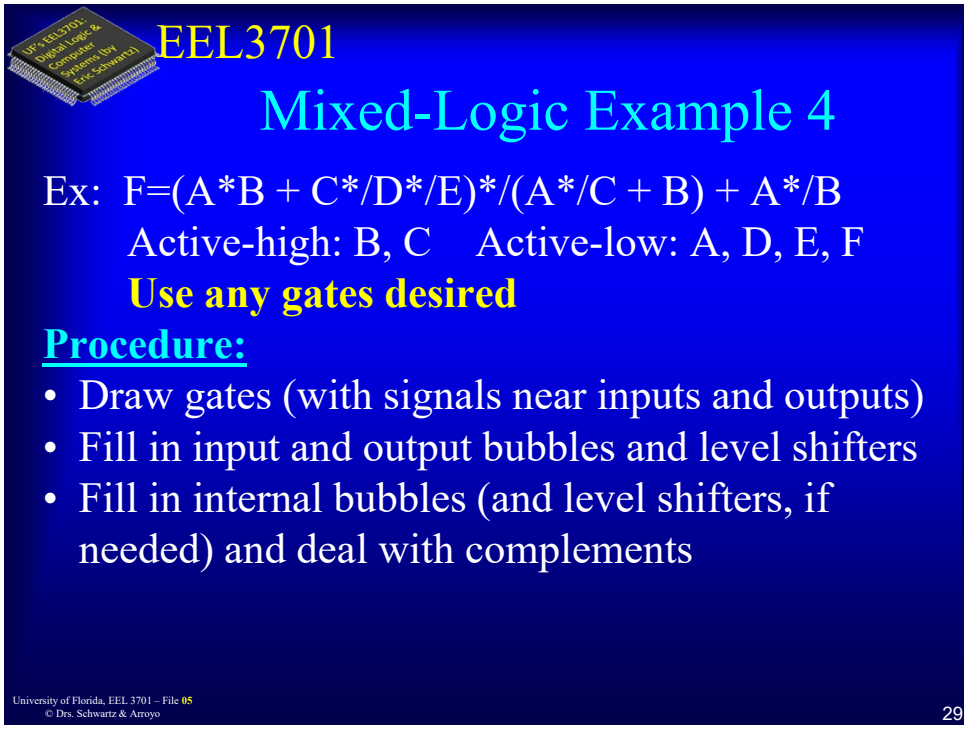
EEL3701
Mixed-Logic Example 4
Ex: F=(A*B + C*/D*/E)*/(A*/C + B) + A*/B
Active-high: B, C Active-low: A, D, E, F
Use any gates desired
Procedure:
• Draw gates (with signals near inputs and outputs)
• Fill in input and output bubbles and level shifters
• Fill in internal bubbles (and level shifters, if needed) and deal with complements
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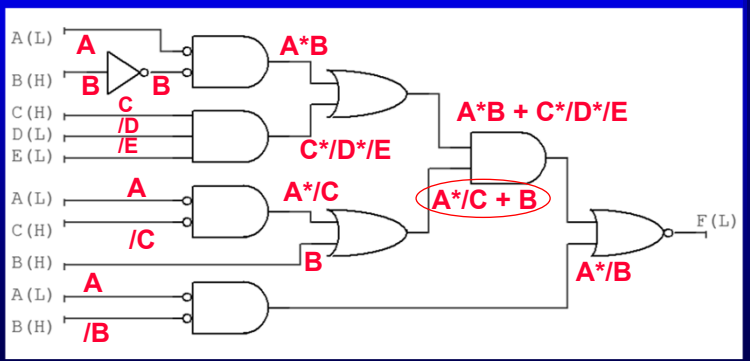
Mixed-Logic Example 4

Ex: F=(A*B + C*/D*/E)*/(A*/C + B) + A*/B Active high: B, C Active Low: A, D, E, F

- Draw I/O with activation levels; Draw gates near I/O to match equation
- Fill in input and output bubbles and level shifters
- **Not quite …**



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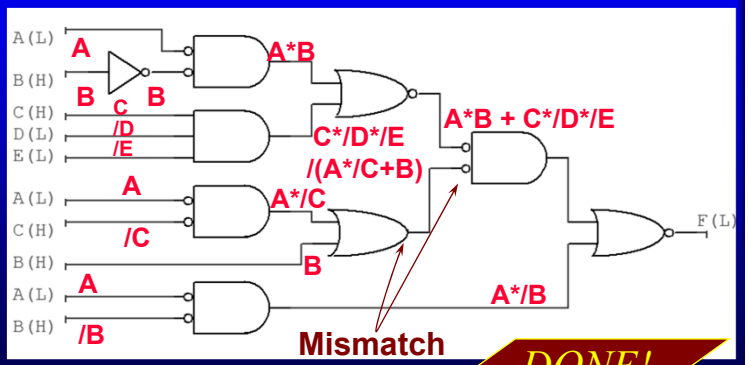
EEL3701

Mixed-Logic Example 4

Ex: F=(A*B + C*/D*/E)*/(A*/C + B) + A*/B Active high: B, C Active Low: A, D, E, F

- Fill in internal bubbles (and level shifters, if needed) and deal with complements



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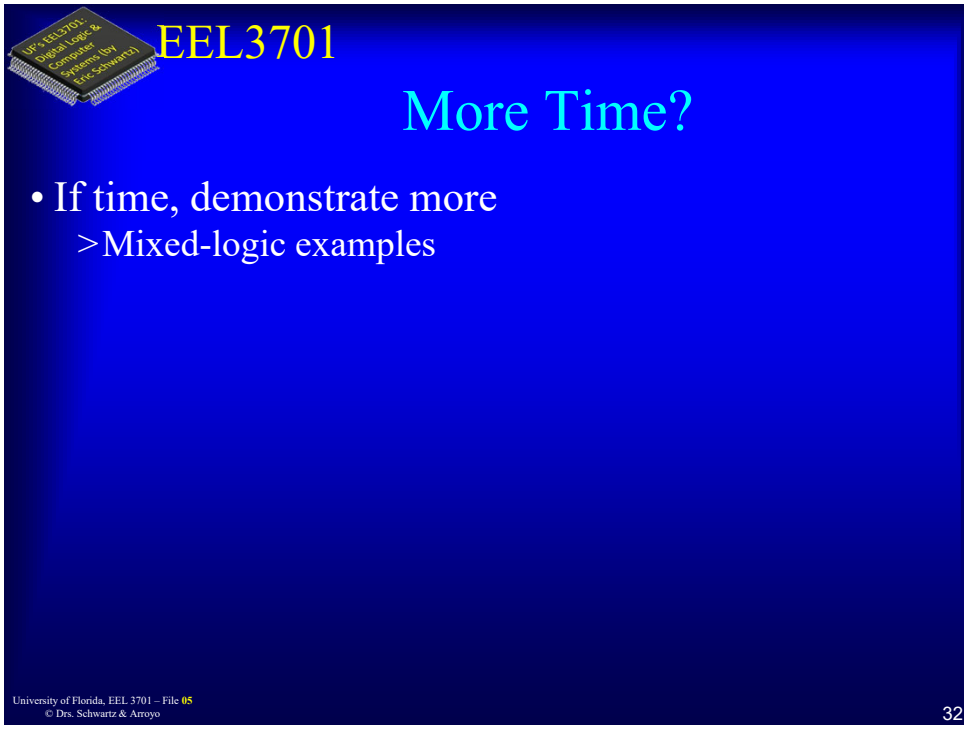

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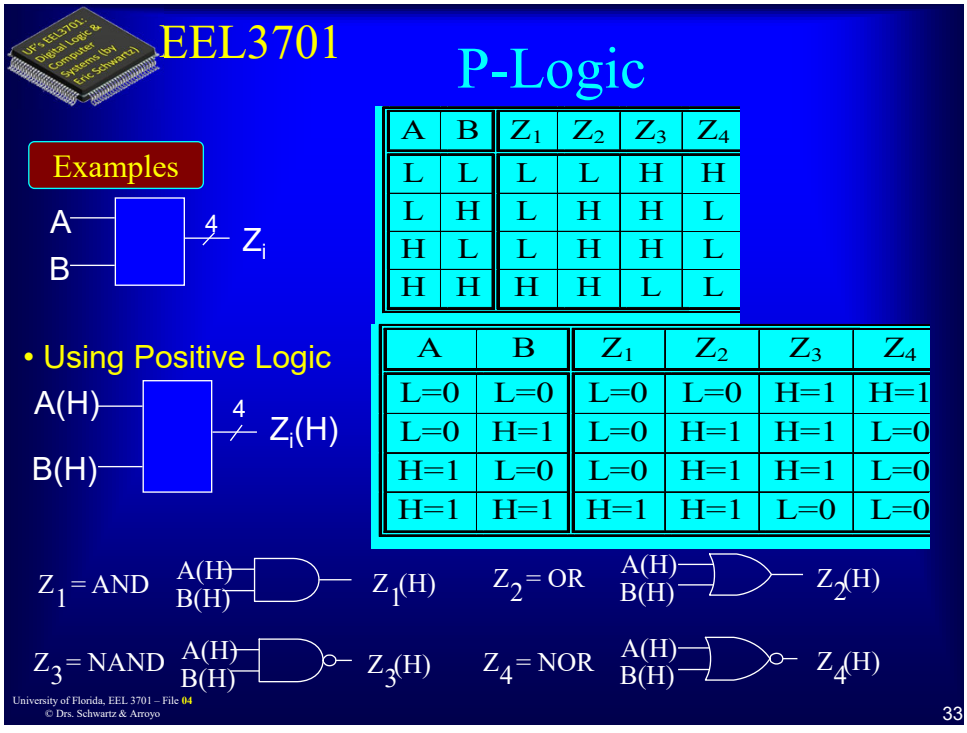

A	B	Z_1	Z_2	Z_3	Z_4
L	L	L	L	H	H
L	H	L	H	H	L
H	L	L	H	H	L
H	H	H	H	L	L

A	B	Z_1	Z_2	Z_3	Z_4
L=0	L=0	L=0	L=0	H=1	H=1
L=0	H=1	L=0	H=1	H=1	L=0
H=1	L=0	L=0	H=1	H=1	L=0
H=1	H=1	H=1	H=1	L=0	L=0

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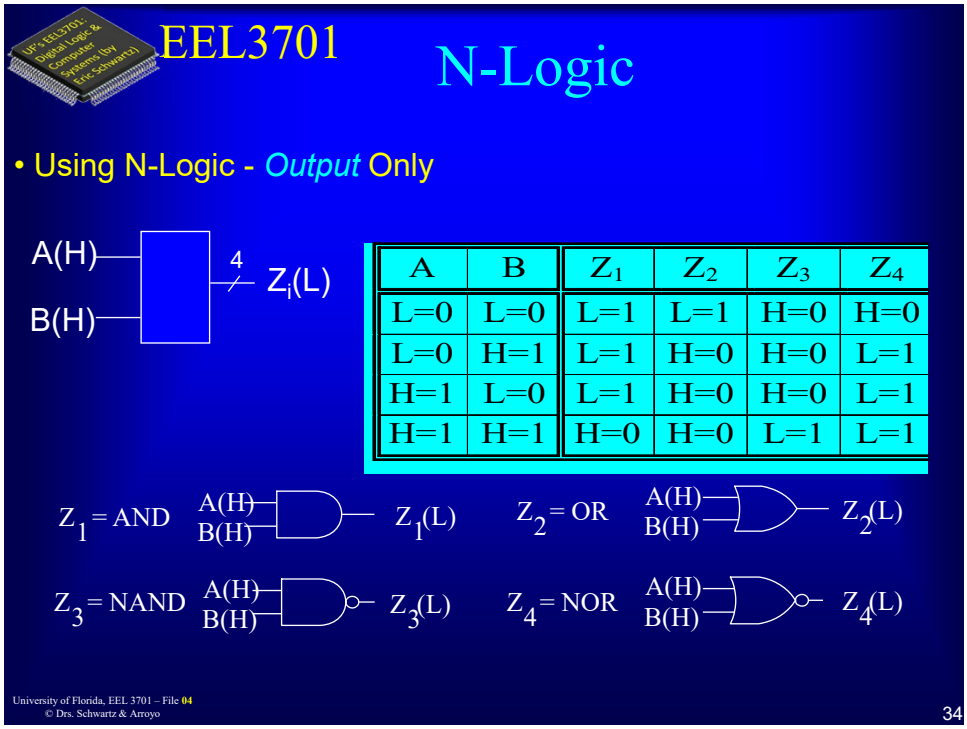
EEL3701
N-Logic
• Using N-Logic - Output Only
A(H)
B(H)
4
Zi(L)
A | B | Z1 | Z2 | Z3 | Z4
L=0 | L=0 | L=1 | L=1 | H=0 | H=0
L=0 | H=1 | L=1 | H=0 | H=0 | L=1
H=1 | L=0 | L=1 | H=0 | H=0 | L=1
H=1 | H=1 | H=0 | H=0 | L=1 | L=1
Z1 = AND
Z1(L)
Z2 = OR
Z2(L)
Z3 = NAND
Z3(L)
Z4 = NOR
Z4(L)
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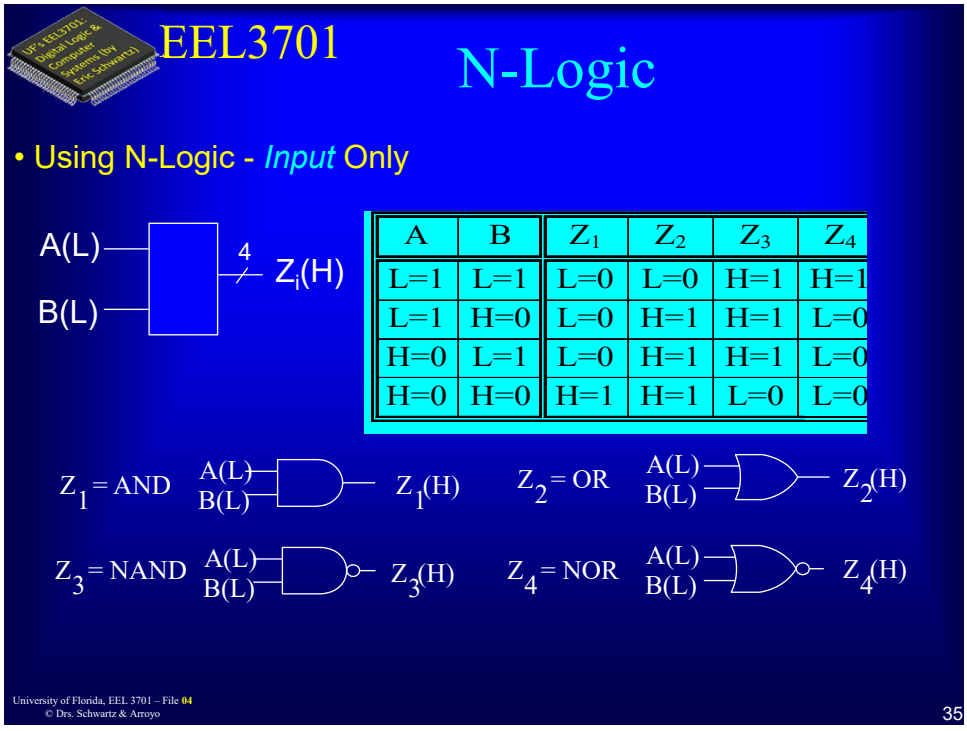
EEL3701
N-Logic
• Using N-Logic - Input Only
A(L)
B(L)
4
Zi(H)
A | B | Z1 | Z2 | Z3 | Z4
L=1 | L=1 | L=0 | L=0 | H=1 | H=1
L=1 | H=0 | L=0 | H=1 | H=1 | L=0
H=0 | L=1 | L=0 | H=1 | H=1 | L=0
H=0 | H=0 | H=1 | H=1 | L=0 | L=0
Z1 = AND
Z1(H)
Z2 = OR
Z2(H)
Z3 = NAND
Z3(H)
Z4 = NOR
Z4(H)
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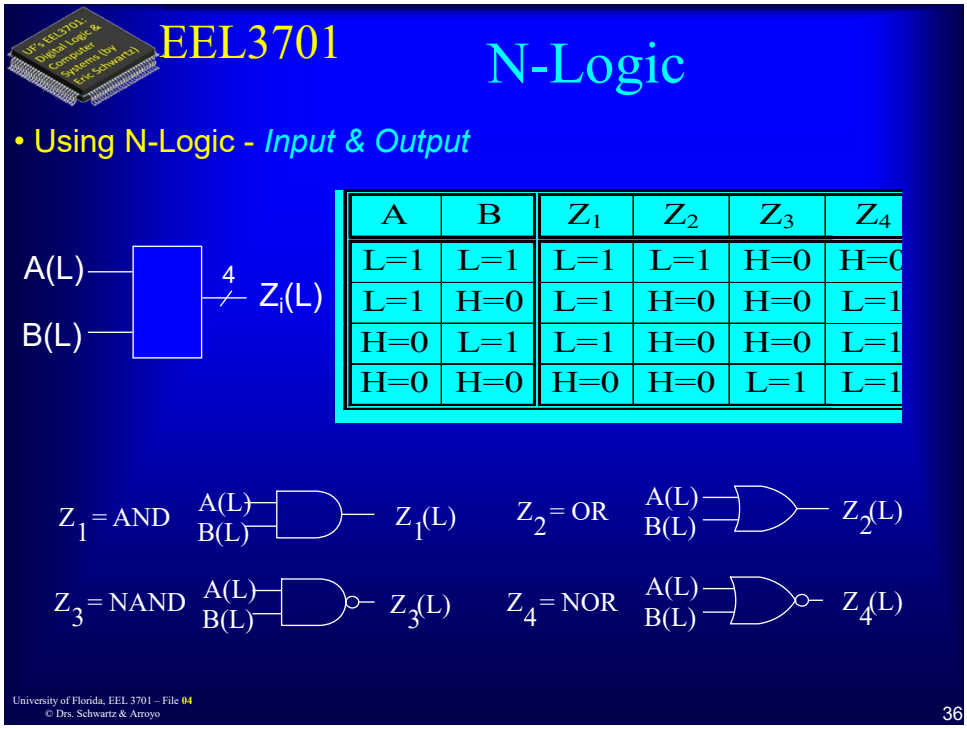
EEL3701
N-Logic
• Using N-Logic - Input & Output
A(L)
B(L)
4
Zi(L)
A | B | Z1 | Z2 | Z3 | Z4
L=1 | L=1 | L=1 | L=1 | H=0 | H=0
L=1 | H=0 | L=1 | H=0 | H=0 | L=1
H=0 | L=1 | L=1 | H=0 | H=0 | L=1
H=0 | H=0 | H=0 | H=0 | L=1 | L=1
Z1 = AND
Z1(L)
Z2 = OR
Z2(L)
Z3 = NAND
Z3(L)
Z4 = NOR
Z4(L)
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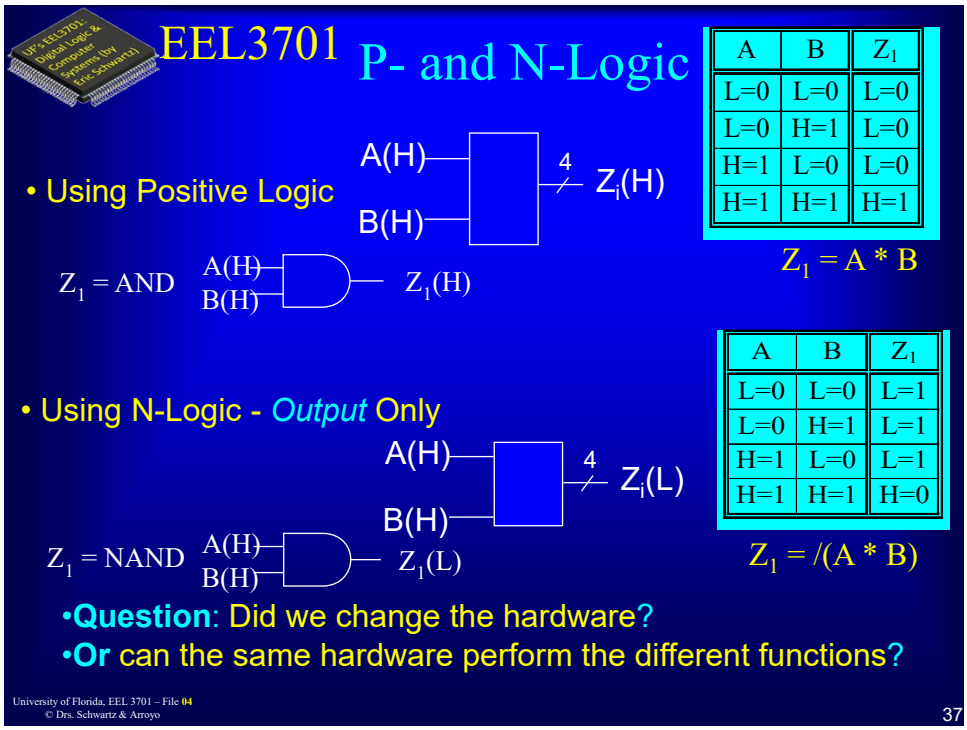
EEL3701
P- and N-Logic
• Using Positive Logic
A(H)
B(H)
4
Zi(H)
Z1 = AND
Z1(H)
A | B | Z1
L=0 | L=0 | L=0
L=0 | H=1 | L=0
H=1 | L=0 | L=0
H=1 | H=1 | H=1
Z1 = A * B
• Using N-Logic - Output Only
Z1 = NAND
Z1(L)
A | B | Z1
L=0 | L=0 | L=1
L=0 | H=1 | L=1
H=1 | L=0 | L=1
H=1 | H=1 | H=0
Z1 = /(A * B)
•Question: Did we change the hardware?
•Or can the same hardware perform the different functions?
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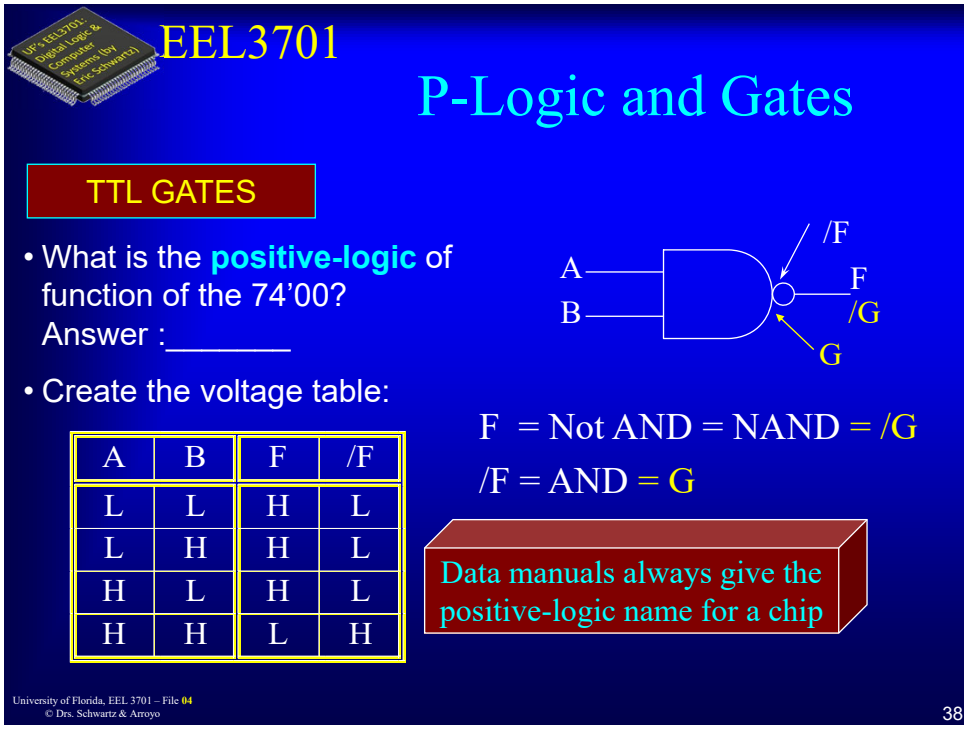

A	B	F	/F
L	L	H	L
L	H	H	L
H	L	H	L
H	H	L	H

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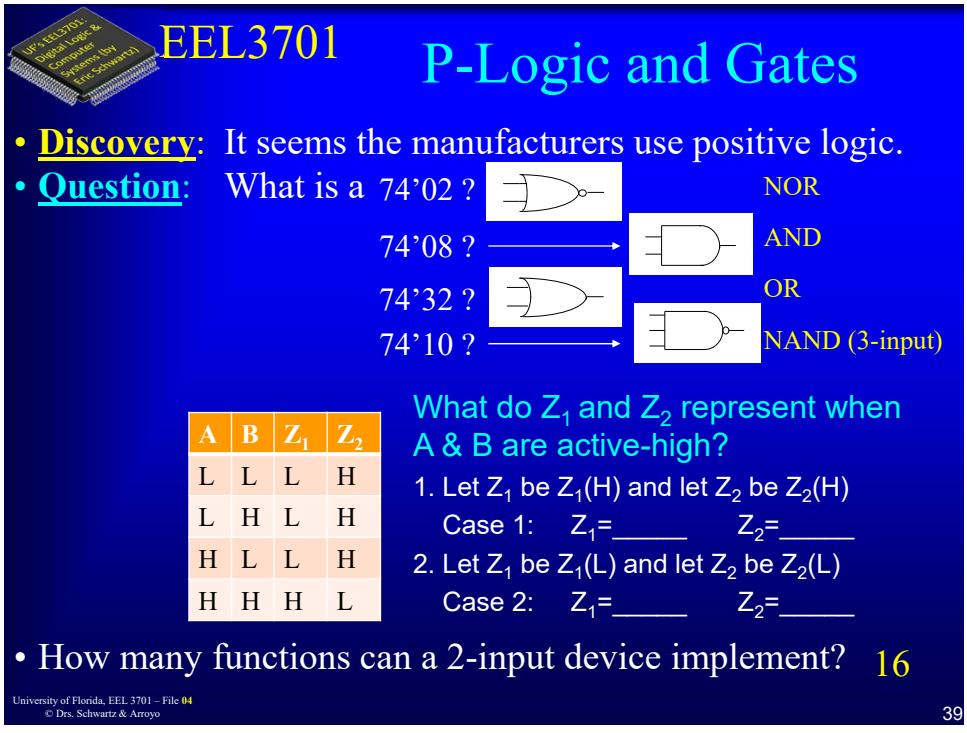

A	B	Z_1	Z_2
L	L	L	H
L	H	L	H
H	L	L	H
H	H	H	L

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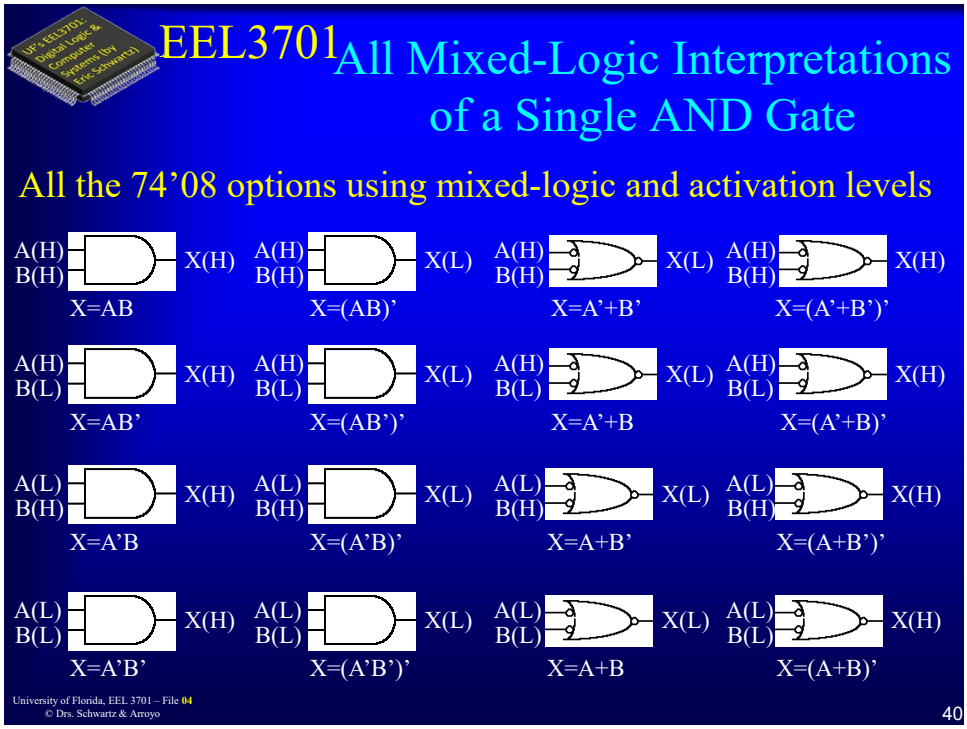
EEL3701
All Mixed-Logic Interpretations of a Single AND Gate
All the 74'08 options using mixed-logic and activation levels
A(H) B(H) X(H) X=AB
A(H) B(H) X(L) X=(AB)'
A(H) B(H) X(L) X=A'+B'
A(H) B(H) X(H) X=(A'+B')'
A(H) B(L) X(H) X=AB'
A(H) B(L) X(L) X=(AB')'
A(H) B(L) X(L) X=A'+B
A(H) B(L) X(H) X=(A'+B)'
A(L) B(H) X(H) X=A'B
A(L) B(H) X(L) X=(A'B)'
A(L) B(H) X(L) X=A+B'
A(L) B(H) X(H) X=(A+B')'
A(L) B(L) X(H) X=A'B'
A(L) B(L) X(L) X=(A'B')'
A(L) B(L) X(L) X=A+B
A(L) B(L) X(H) X=(A+B)'
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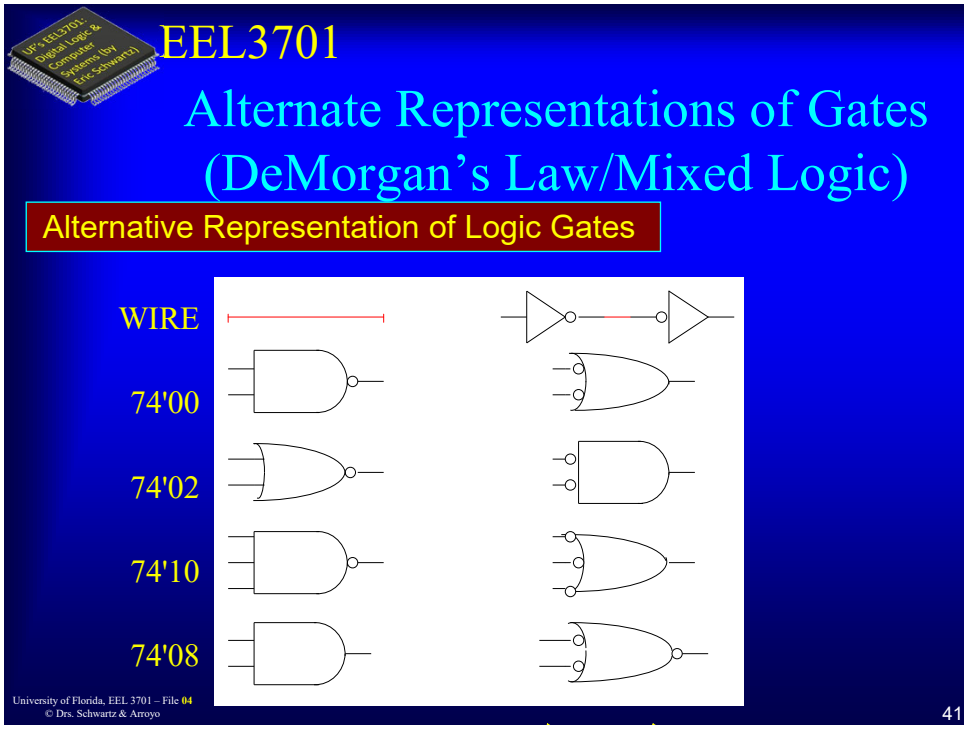
EEL3701
Alternate Representations of Gates (DeMorgan's Law/Mixed Logic)
Alternative Representation of Logic Gates
WIRE
74'00
74'02
74'10
74'08
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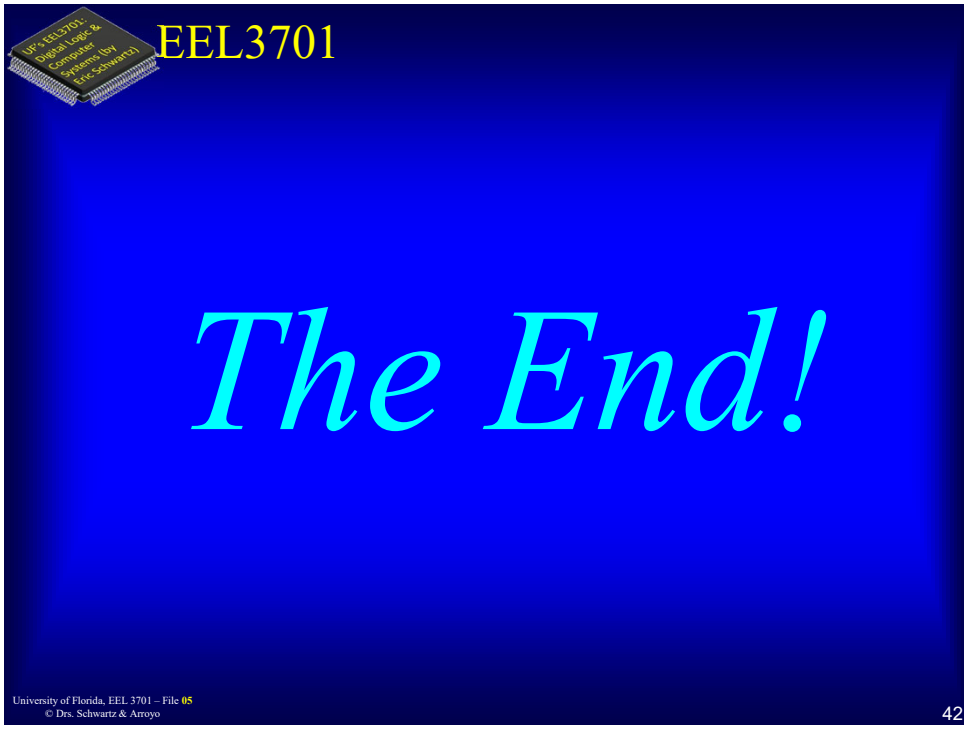
EEL3701
The End!
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